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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,769	08/05/2003	Todd W. Goforth	IGT1P095/P000813-001	1651

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EXAMINER	
WONG, JEFFREY KEITH	

ART UNIT	PAPER NUMBER
3714	

NOTIFICATION DATE	DELIVERY MODE
08/12/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@wavsip.com

Office Action Summary	Application No.	Applicant(s)	
	10/635,769	GOFORTH ET AL.	
	Examiner	Art Unit	
	Jeffrey K. Wong	3714	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 23-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/4/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Application

1. This Office-Action acknowledges the Amendment filed on 6/4/2010 and is a response to said Amendment.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-13, 15-17, 19-20, 23, 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loose, PGPUB 2004/0161115 (Loose) and Neal et al., US 6,237,057 (Neal)

Regarding Claim 1.

Loose teaches a wager-based gaming machine comprising: one or more speakers(para 21); a master gaming controller adapted to process and facilitate the presentation of a wager- based game(para 3); a digital sound system comprising: at least one memory unit storing data(para 7), wherein said data comprises one or more wave files, one or more sets of wave table data, or both (para 21. While Loose does not explicitly teach of wave files, it is implied that the stored data comprises wave files), and a digital signal processor configured to produce audio output for said one or more

speakers(para 7), wherein said digital signal processor is adapted to perform at least one function selected from the group consisting of generating original audio output and modifying existing sound files(para 7); a programmable logic device interposed between the master gaming controller (fig 3) and the digital sound system (para 28. In this case, the CPU communicates with the digital sound system through elem 32. It can be implied that the interface may be any suitable interface such as a programmable logic device can receive instructions. It is also well known that interfaces can comprise of programmable logic devices.); and wherein said programmable logic device converts instructions from said master gaming controller to instructions that can be executed by said digital signal processor(para 37).

Loose failed to disclose where said programmable logic device and said master gaming controller are communicatively coupled by a control line, an address line, and a data line, said control line and said address line configured such that information can only be sent from the master gaming controller to the programmable logic device, and said data line configured such that data bits may be sent in both directions.

However, Neal teaches that several different bus designs have been developed for interconnecting the various computer components and optional devices, such as additional memory (RAM), sound cards, telephone modems, etc. One improvement was by adding more data and address lines, new interrupt lines, and direct memory-access (DMA) control lines, to create the well-known AT bus, which is also referred to as the Industry Standard Architecture (ISA) bus. (Col 1, lines 14-50) because such

communication methods would allow additional peripheral devices to be added to the system (Col 3, lines 16-24).

Therefore, it would have been obvious to implement Neal's well known teachings of using address, control, and data lines for communicating between computer components of Loose's invention because it would allows addition of peripheral devices to be added to the system as taught by Neal.

Regarding Claims 2, 15, 19.

Loose teaches wherein the programmable logic device forms an event sequencer interposed between the master gaming controller and the digital signal processor (para 37. elem 32 can be viewed as an event sequencer since an event sequencer can receive instructions)

Regarding Claims 3, 13.

Loose teaches wherein said digital signal processor is configured to alter musical or tonal parameters while a sound file is playing(para 28. DSPs can be used to alter

Regarding Claim 4, 23.

Loose teaches wherein said digital signal processor is configured to synthesize music in real-time(para 28. DSPs can be used to synthesize music).

Regarding Claim 9, 27.

Loose teaches wherein said digital sound system comprises additional memory for storing audio processing algorithms for execution on the digital signal processor(para 14).

Regarding Claim 10, 28.

Loose discloses wherein said event sequencer is installed in a manner that prevents the digital signal processor from effecting operation of the master gaming controller(para 28).

Regarding Claim 11.

Loose teaches a wager-based gaming machine, comprising:

a central processing unit (para 7) adapted to process and facilitate the presentation of a wager- based game(para 3); a programmable logic device separate from and connected to said central processing unit(fig 3 and para 28); and a digital signal processor adapted to generate and control digital output(para 7), said digital signal processor being separate from and connected to said programmable logic device(fig 3), wherein said programmable logic device is interposed between said central processing unit and said digital signal processor(fig 3), and wherein said programmable logic device converts instructions from said central processing unit to instructions that can be executed by said digital signal processor(para 37).

Loose failed to disclose where said programmable logic device and said master gaming controller are communicatively coupled by a control line, an address line, and a data line, said control line and said address line configured such that information can only be sent from the master gaming controller to the programmable logic device, and said data line configured such that data bits may be sent in both directions.

However, Neal teaches that several different bus designs have been developed for interconnecting the various computer components and optional devices, such as additional memory (RAM), sound cards, telephone modems, etc. One improvement was by adding more data and address lines, new interrupt lines, and direct memory-access (DMA) control lines, to create the well-known AT bus, which is also referred to as the Industry Standard Architecture (ISA) bus. (Col 1, lines 14-50) because such communication methods would allow additional peripheral devices to be added to the system (Col 3, lines 16-24).

Therefore, it would have been obvious to implement Neal's well known teachings of using address, control, and data lines for communicating between computer components of Loose's invention because it would allows addition of peripheral devices to be added to the system as taught by Neal.

Regarding Claim 12.

Loose teaches wherein said digital signal processor is adapted to generate and control audio output for one or more speakers(para 7).

Regarding Claim 16, 20.

Loose teaches wherein said central processing unit comprises a master gaming controller(para 7. The CPU is used for controlling the game system).

Regarding Claim 17.

Loose teaches a method of providing sound in a wager-based gaming machine, comprising(Abstract), receiving, at a programmable logic device, CPU instructions from a central processing unit (para 10. The first control module includes a main processor for sending audio information that controls audio output from the gaming machine), said central processing unit being configured to process and facilitate presentation of a wager-based game (para 10. The first control module includes a main processor for randomly selecting one of a plurality of outcomes of the gaming machine in response to a wager amount);

converting said CPU instructions to DSP instructions that can be executed by a digital signal processor (para 28. The main CPU 16 communicates with a DSP 34 via an interface 32, which places instructions from the main CPU 16 in a proper format for the DSP 34.);

generating and controlling audio output for one or more speakers (para 10), responsive to the DSP instructions, with the digital signal processor, said digital signal processor being separate from and connected to said programmable logic device (fig 3), the programmable logic device being separate from and connected to the central

processing unit (fig 3); wherein said programmable logic device is interposed between said central processing unit and said digital signal processor(fig 3).

Loose failed to disclose where said programmable logic device and said master gaming controller are communicatively coupled by a control line, an address line, and a data line, said control line and said address line configured such that information can only be sent from the master gaming controller to the programmable logic device, and said data line configured such that data bits may be sent in both directions.

However, Neal teaches that several different bus designs have been developed for interconnecting the various computer components and optional devices, such as additional memory (RAM), sound cards, telephone modems, etc. One improvement was by adding more data and address lines, new interrupt lines, and direct memory-access (DMA) control lines, to create the well-known AT bus, which is also referred to as the Industry Standard Architecture (ISA) bus. (Col 1, lines 14-50) because such communication methods would allow additional peripheral devices to be added to the system (Col 3, lines 16-24).

Therefore, it would have been obvious to implement Neal's well known teachings of using address, control, and data lines for communicating between computer components of Loose's invention because it would allows addition of peripheral devices to be added to the system as taught by Neal.

Claims 5-8, 14, 18, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loose, PGPUB 2004/0161115 (Loose) and Neal et al, US 6,237,057 (Neal) as

applied to the claims above, and in further view of Prezby, PGPUB 2003/0100359 (Prezby).

Regarding Claims 5, 14, 18.

Loose and Neal failed to teach wherein said digital signal processor is configured to provide audio output tailored to a player currently using the gaming machine. However, Pryzby teaches of a slot game where audio can be tailor to a player using the machine based on their recorded voice (para 45) as means of generating an enhanced audio output which will attract frequent play and generate more excitement associated with the game (para 4)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the tailored audio output of Pryzby's teachings with Loose's and Neal's invention as means of attracting more frequent play and generating more excitement associated with the game as taught by Pryzby.

Regarding Claim 6, 24.

Pryzby also teaches wherein said digital output is tailored by at least one or more parameters selected from the group consisting of language selection, gender selection, accent selection, and style selection(para 40-41. In this case, the style selection can be viewed as the music style being played upon a player's response).

Regarding Claim 7, 25.

Pryzby also teaches wherein said digital signal processor is configured to recognize

speech used by a player at or near the gaming machine(para 40).

Regarding Claim 8, 26.

Pryzby also teaches wherein said digital sound system further comprises a microphone, as well as speech recognition logic implemented on the digital signal processor(para 41).

Response to Arguments

3. Applicant's arguments with respect to claims 1-20 and 23-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey K. Wong whose telephone number is (571)270-3003. The examiner can normally be reached on M-Th 8:30am-7:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Hotaling can be reached on (571)272-4437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John M Hotaling II/
Primary Examiner, Art Unit 3714

JKW